FIG. 1

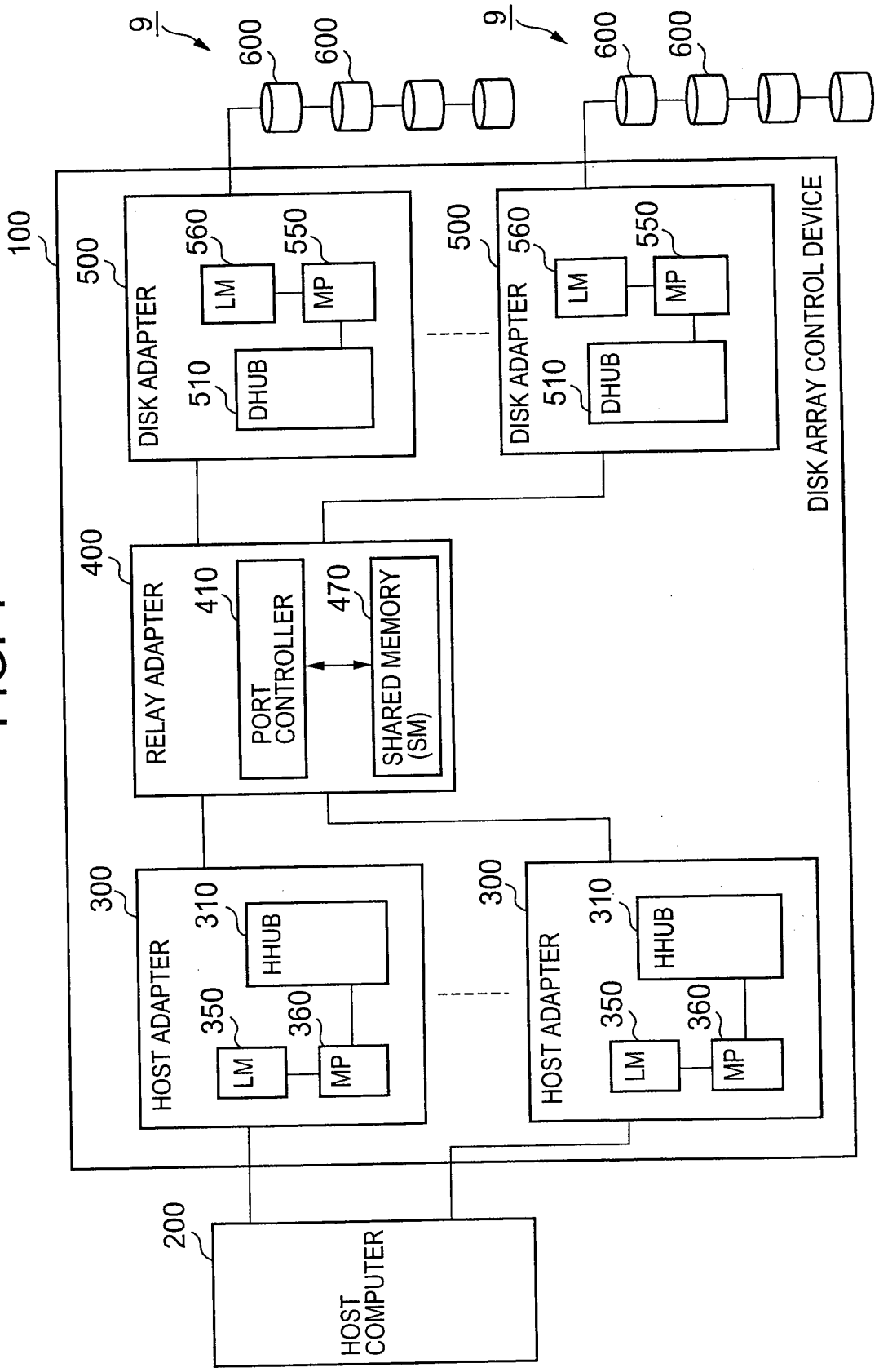

9
600
600
9
600
600
100
DISK ARRAY CONTROL DEVICE
500
DISK ADAPTER
560
LM
550
MP
510
DHUB
500
DISK ADAPTER
560
LM
550
MP
510
DHUB
400
RELAY ADAPTER
410
PORT CONTROLLER
470
SHARED MEMORY (SM)
300
HOST ADAPTER
310
HHUB
350
LM
360
MP
300
HOST ADAPTER
310
HHUB
350
LM
360
MP
200
HOST COMPUTER

FIG. 2

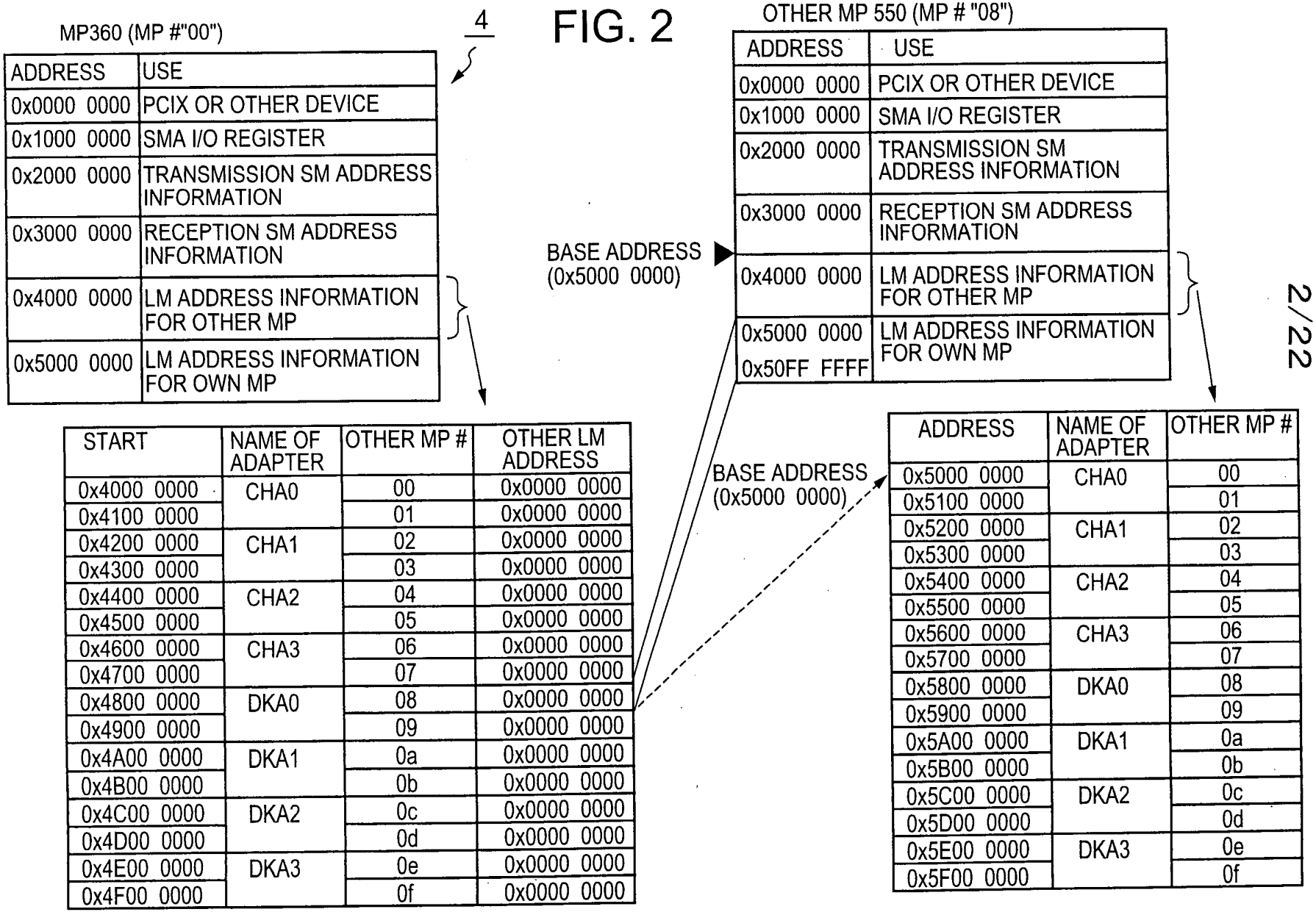

4
MP360 (MP #"00")
ADDRESS
USE
0x0000 0000
PCIX OR OTHER DEVICE
0x1000 0000
SMA I/O REGISTER
0x2000 0000
TRANSMISSION SM ADDRESS INFORMATION
0x3000 0000
RECEPTION SM ADDRESS INFORMATION
0x4000 0000
LM ADDRESS INFORMATION FOR OTHER MP
0x5000 0000
LM ADDRESS INFORMATION FOR OWN MP
OTHER MP 550 (MP # "08")
ADDRESS
USE
0x0000 0000
PCIX OR OTHER DEVICE
0x1000 0000
SMA I/O REGISTER
0x2000 0000
TRANSMISSION SM ADDRESS INFORMATION
0x3000 0000
RECEPTION SM ADDRESS INFORMATION
BASE ADDRESS (0x5000 0000)
0x4000 0000
LM ADDRESS INFORMATION FOR OTHER MP
0x5000 0000
0x50FF FFFF
LM ADDRESS INFORMATION FOR OWN MP
START
NAME OF ADAPTER
OTHER MP #
OTHER LM ADDRESS
0x4000 0000
CHA0
00
0x0000 0000
0x4100 0000
01
0x0000 0000
0x4200 0000
CHA1
02
0x0000 0000
0x4300 0000
03
0x0000 0000
0x4400 0000
CHA2
04
0x0000 0000
0x4500 0000
05
0x0000 0000
0x4600 0000
CHA3
06
0x0000 0000
0x4700 0000
07
0x0000 0000
0x4800 0000
DKA0
08
0x0000 0000
0x4900 0000
09
0x0000 0000
0x4A00 0000
DKA1
0a
0x0000 0000
0x4B00 0000
0b
0x0000 0000
0x4C00 0000
DKA2
0c
0x0000 0000
0x4D00 0000
0d
0x0000 0000
0x4E00 0000
DKA3
0e
0x0000 0000
0x4F00 0000
0f
0x0000 0000
BASE ADDRESS (0x5000 0000)
ADDRESS
NAME OF ADAPTER
OTHER MP #
0x5000 0000
CHA0
00
0x5100 0000
01
0x5200 0000
CHA1
02
0x5300 0000
03
0x5400 0000
CHA2
04
0x5500 0000
05
0x5600 0000
CHA3
06
0x5700 0000
07
0x5800 0000
DKA0
08
0x5900 0000
09
0x5A00 0000
DKA1
0a
0x5B00 0000
0b
0x5C00 0000
DKA2
0c
0x5D00 0000
0d
0x5E00 0000
DKA3
0e
0x5F00 0000
0f

FIG. 3

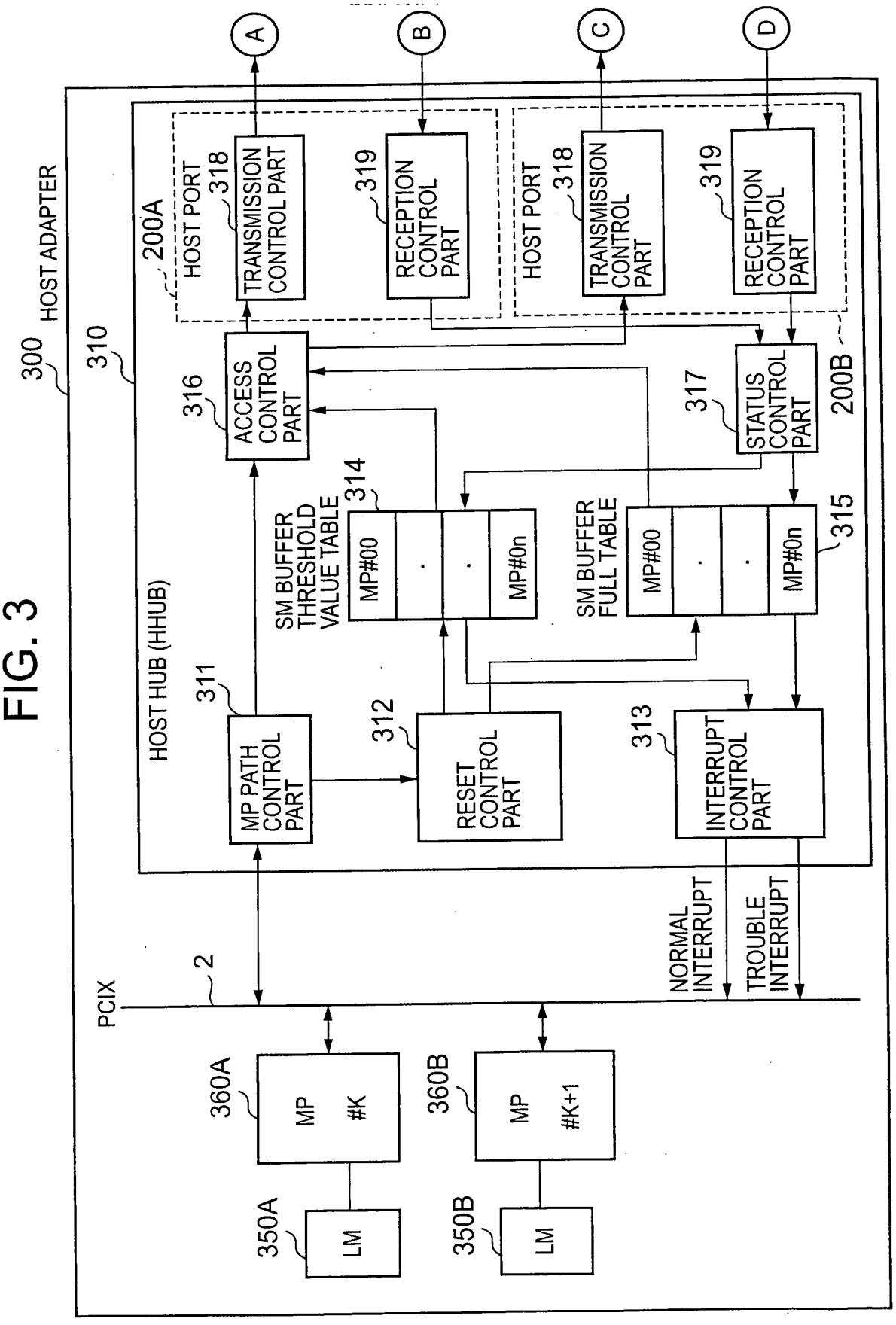

300
HOST ADAPTER
310
HOST HUB (HHUB)
200A
HOST PORT
318
TRANSMISSION CONTROL PART
319
RECEPTION CONTROL PART
HOST PORT
318
TRANSMISSION CONTROL PART
319
RECEPTION CONTROL PART
200B
316
ACCESS CONTROL PART
317
STATUS CONTROL PART
314
SM BUFFER THRESHOLD VALUE TABLE
MP#00
MP#0n
SM BUFFER FULL TABLE
MP#00
MP#0n
315
311
MP PATH CONTROL PART
312
RESET CONTROL PART
313
INTERRUPT CONTROL PART
A
B
C
D
2
PCIX
NORMAL INTERRUPT
TROUBLE INTERRUPT
360A
MP #K
360B
MP #K+1
350A
LM
350B
LM

FIG. 4

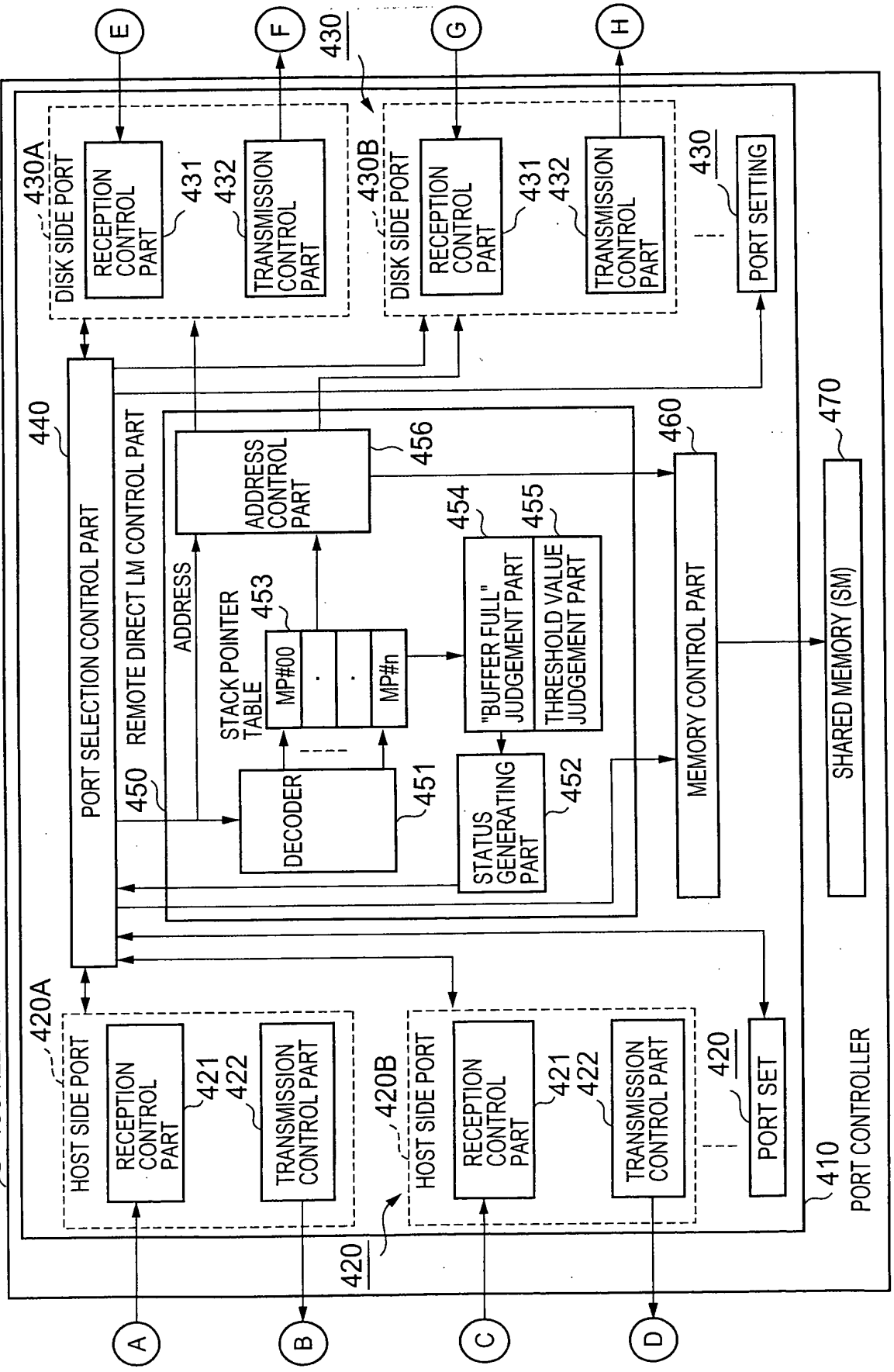

400 RELAY ADAPTER
410 PORT CONTROLLER
420 HOST SIDE PORT
420A
420B
RECEPTION CONTROL PART
421
TRANSMISSION CONTROL PART
422
PORT SET
430 DISK SIDE PORT
430A
430B
431
432
PORT SETTING
440 PORT SELECTION CONTROL PART
450 REMOTE DIRECT LM CONTROL PART
451 DECODER
452 STATUS GENERATING PART
453 STACK POINTER TABLE
MP#00
MP#n
ADDRESS
456 ADDRESS CONTROL PART
454 "BUFFER FULL" JUDGEMENT PART
455 THRESHOLD VALUE JUDGEMENT PART
460 MEMORY CONTROL PART
470 SHARED MEMORY (SM)
A
B
C
D
E
F
G
H

FIG. 5

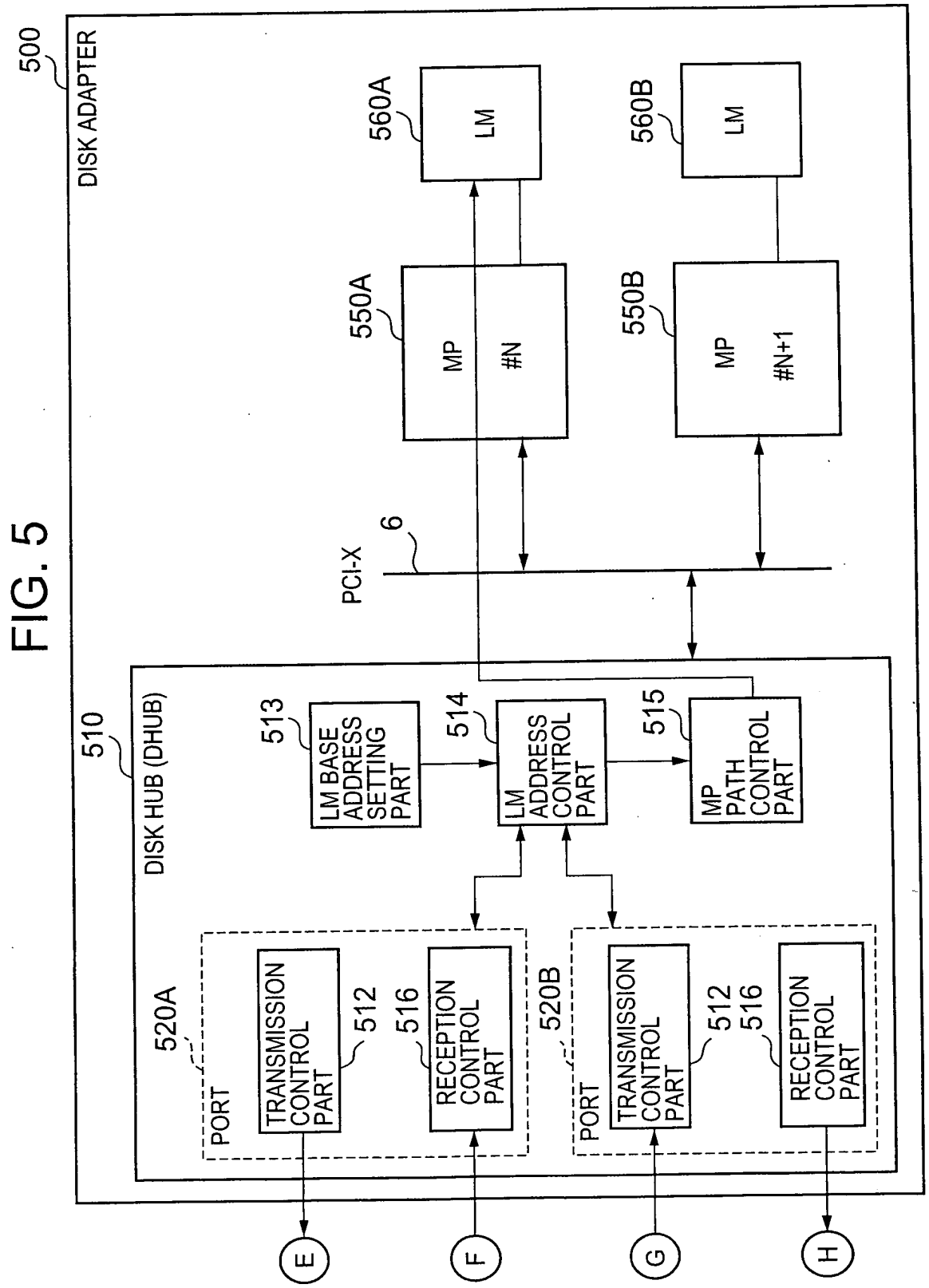

500
DISK ADAPTER
560A
LM
560B
LM
550A
MP
#N
550B
MP
#N+1
PCI-X
6
510
DISK HUB (DHUB)
513
LM BASE ADDRESS SETTING PART
514
LM ADDRESS CONTROL PART
515
MP PATH CONTROL PART
520A
PORT
TRANSMISSION CONTROL PART
512
516
RECEPTION CONTROL PART
520B
PORT
TRANSMISSION CONTROL PART
512
516
RECEPTION CONTROL PART
E
F
G
H

FIG. 6

FIG. 7

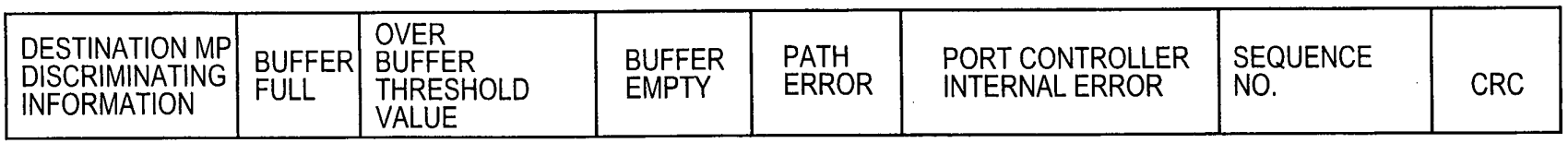


FIG. 8

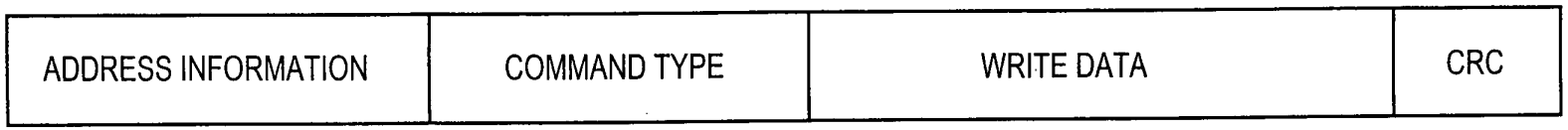


FIG. 9

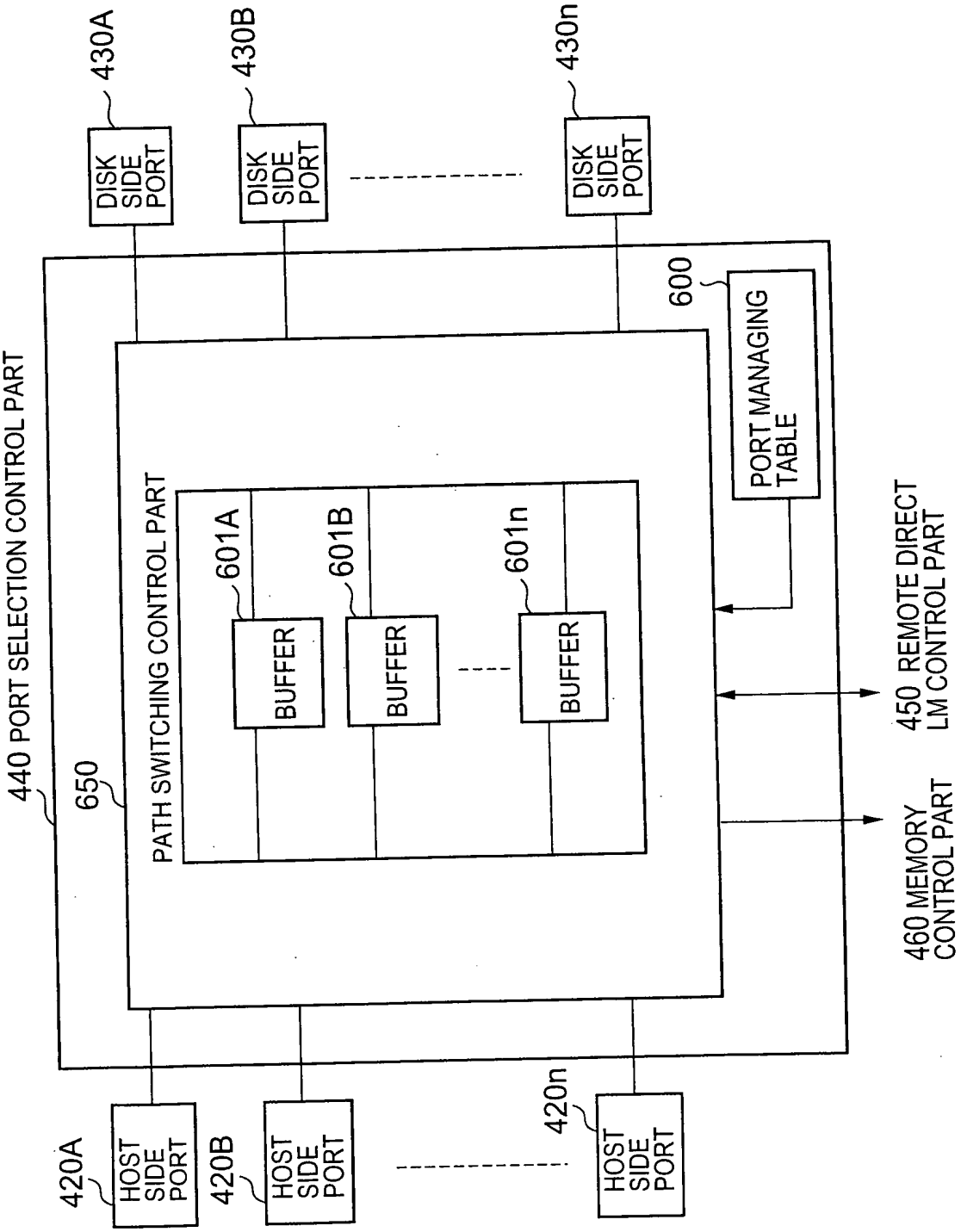

440 PORT SELECTION CONTROL PART
650
PATH SWITCHING CONTROL PART
601A
601B
601n
BUFFER
BUFFER
BUFFER
600
PORT MANAGING TABLE
430A
430B
430n
DISK SIDE PORT
DISK SIDE PORT
DISK SIDE PORT
420A
420B
420n
HOST SIDE PORT
HOST SIDE PORT
HOST SIDE PORT
450 REMOTE DIRECT LM CONTROL PART
460 MEMORY CONTROL PART

FIG. 10

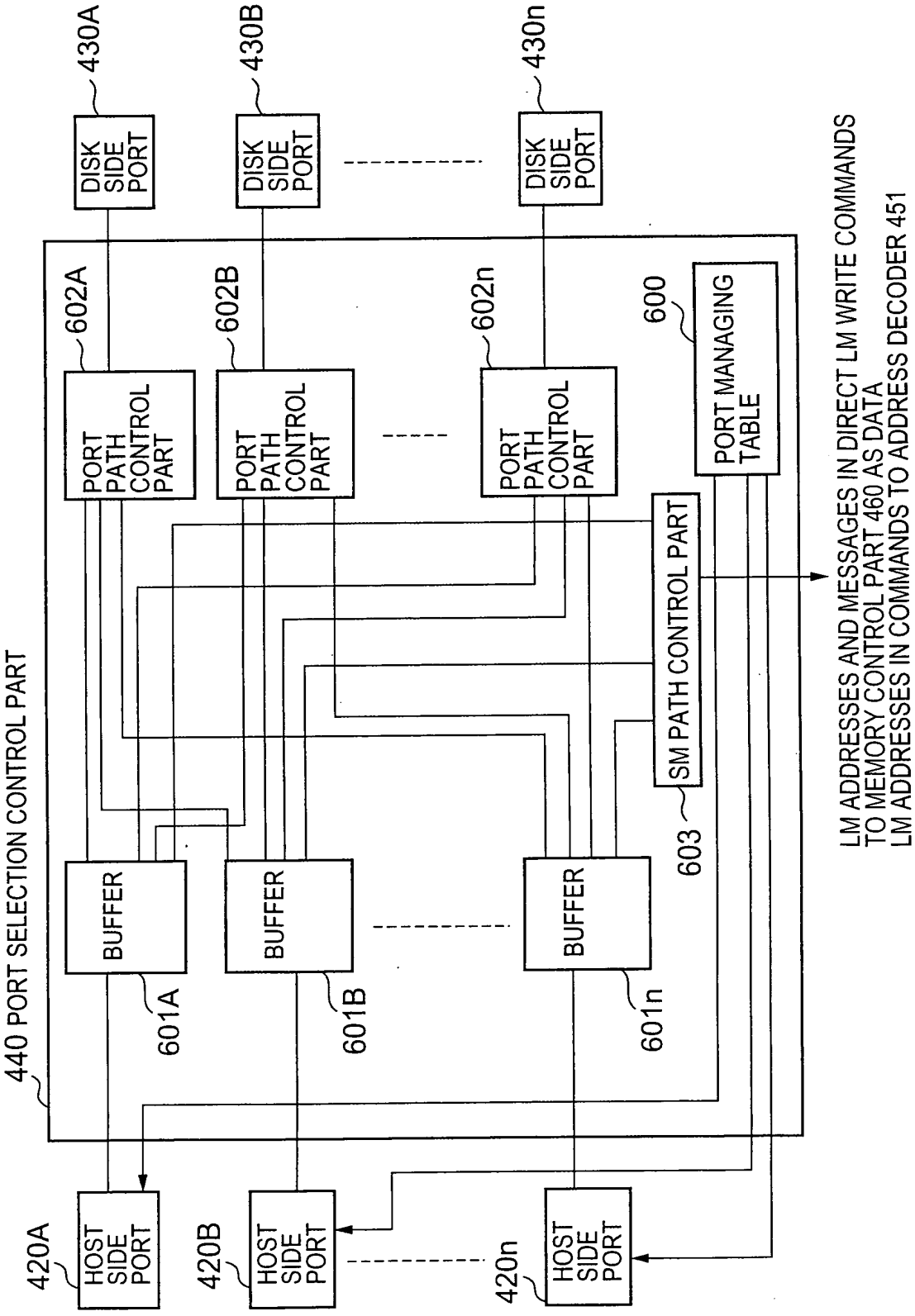

440 PORT SELECTION CONTROL PART
430A
430B
430n
DISK SIDE PORT
602A
602B
602n
PORT PATH CONTROL PART
600
PORT MANAGING TABLE
SM PATH CONTROL PART
603
BUFFER
601A
601B
601n
420A
420B
420n
HOST SIDE PORT
LM ADDRESSES AND MESSAGES IN DIRECT LM WRITE COMMANDS
TO MEMORY CONTROL PART 460 AS DATA
LM ADDRESSES IN COMMANDS TO ADDRESS DECODER 451

FIG. 11

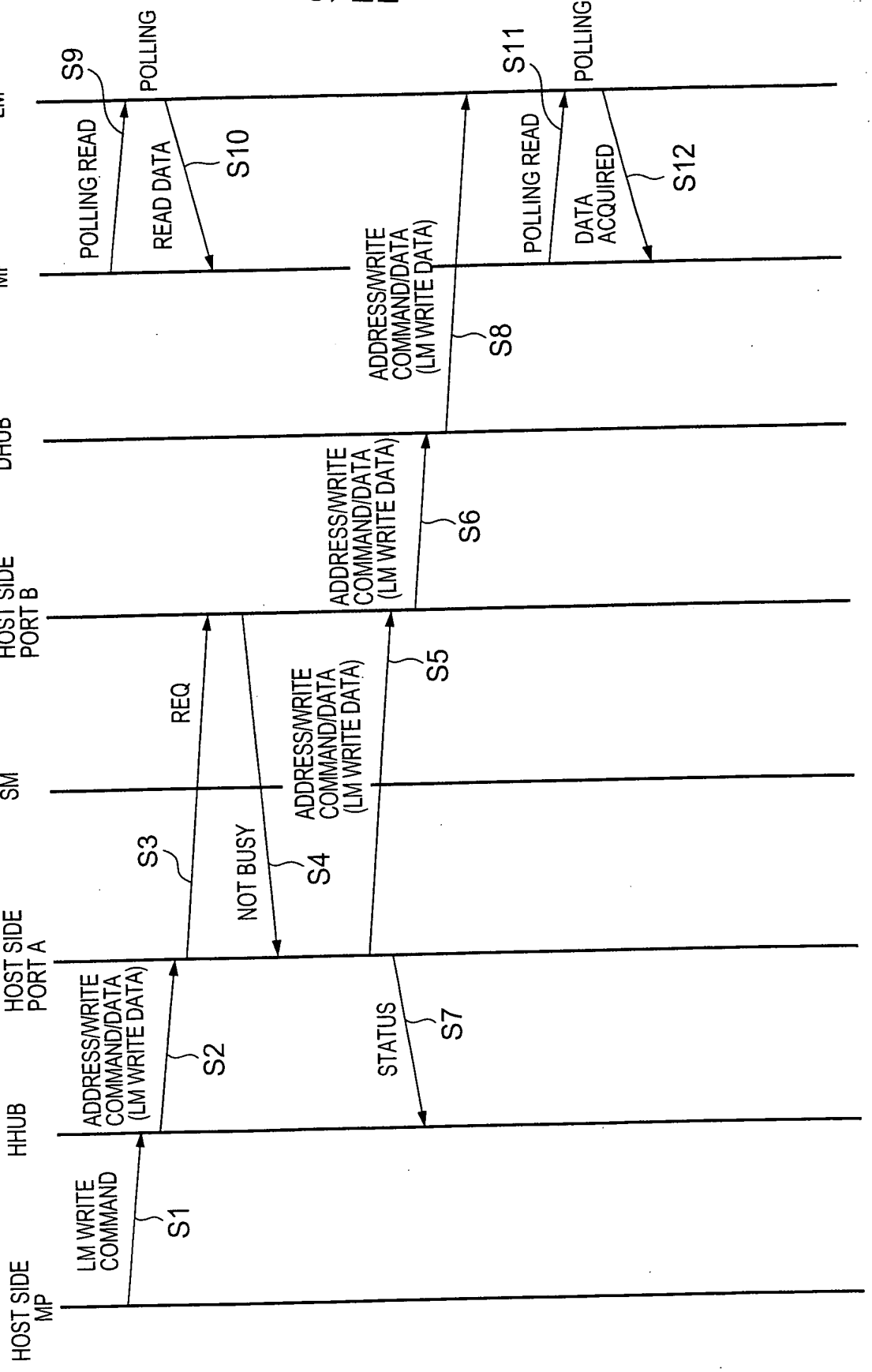

HOST SIDE MP
HHUB
HOST SIDE PORT A
SM
HOST SIDE PORT B
DHUB
MP
LM
LM WRITE COMMAND
S1
ADDRESS/WRITE COMMAND/DATA (LM WRITE DATA)
S2
REQ
S3
NOT BUSY
S4
ADDRESS/WRITE COMMAND/DATA (LM WRITE DATA)
S5
ADDRESS/WRITE COMMAND/DATA (LM WRITE DATA)
S6
STATUS
S7
ADDRESS/WRITE COMMAND/DATA (LM WRITE DATA)
S8
S9
POLLING
POLLING READ
READ DATA
S10
S11
POLLING
POLLING READ
DATA ACQUIRED
S12

FIG. 12

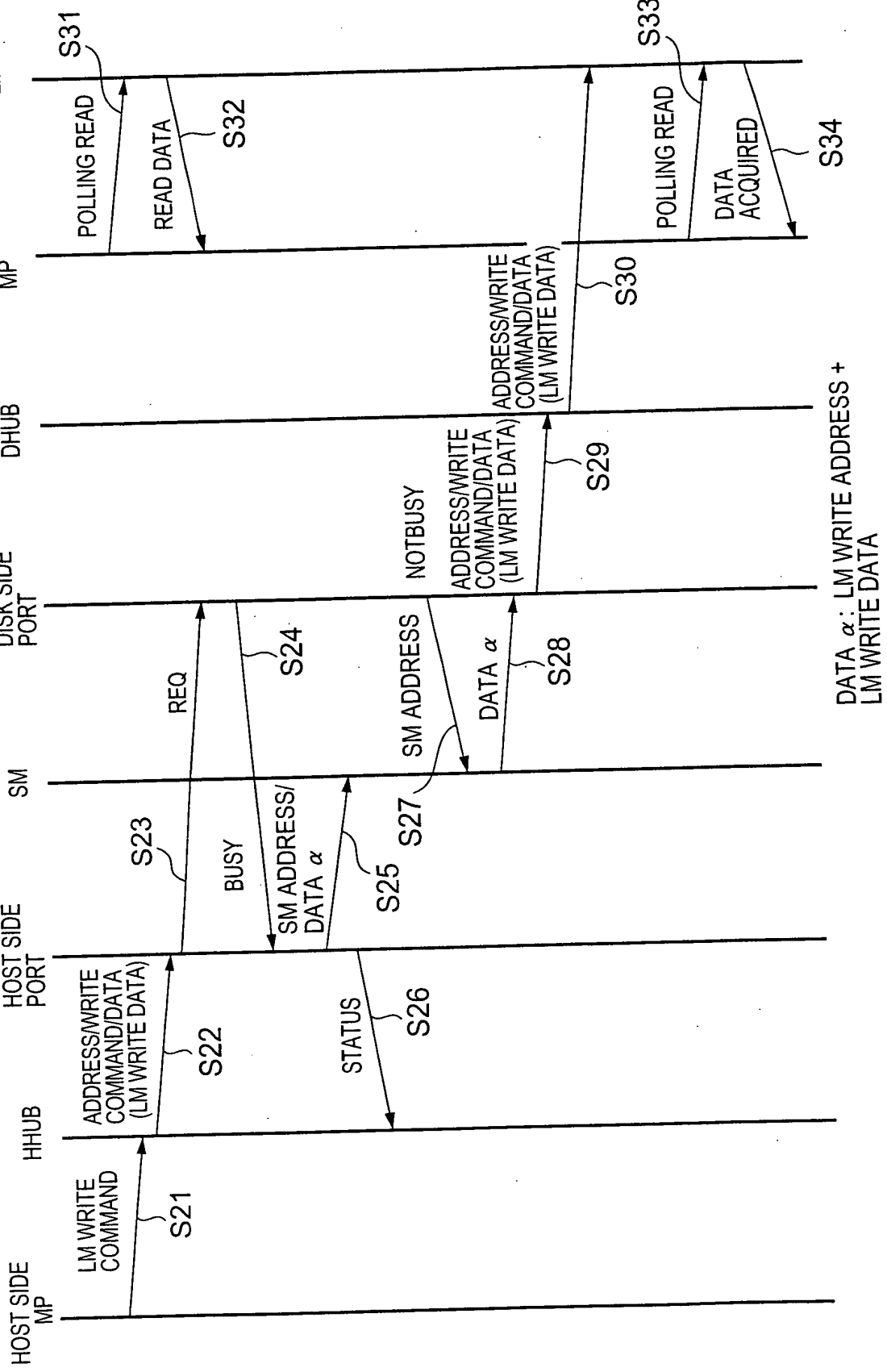

HOST SIDE MP
HHUB
HOST SIDE PORT
SM
DISK SIDE PORT
DHUB
DISK SIDE MP
LM
LM WRITE COMMAND
S21
ADDRESS/WRITE COMMAND/DATA (LM WRITE DATA)
S22
REQ
S23
BUSY
S24
SM ADDRESS/ DATA α
S25
STATUS
S26
SM ADDRESS
S27
DATA α
S28
NOTBUSY
ADDRESS/WRITE COMMAND/DATA (LM WRITE DATA)
S29
ADDRESS/WRITE COMMAND/DATA (LM WRITE DATA)
S30
POLLING READ
S31
READ DATA
S32
POLLING READ
S33
DATA ACQUIRED
S34
DATA α: LM WRITE ADDRESS + LM WRITE DATA

FIG. 13

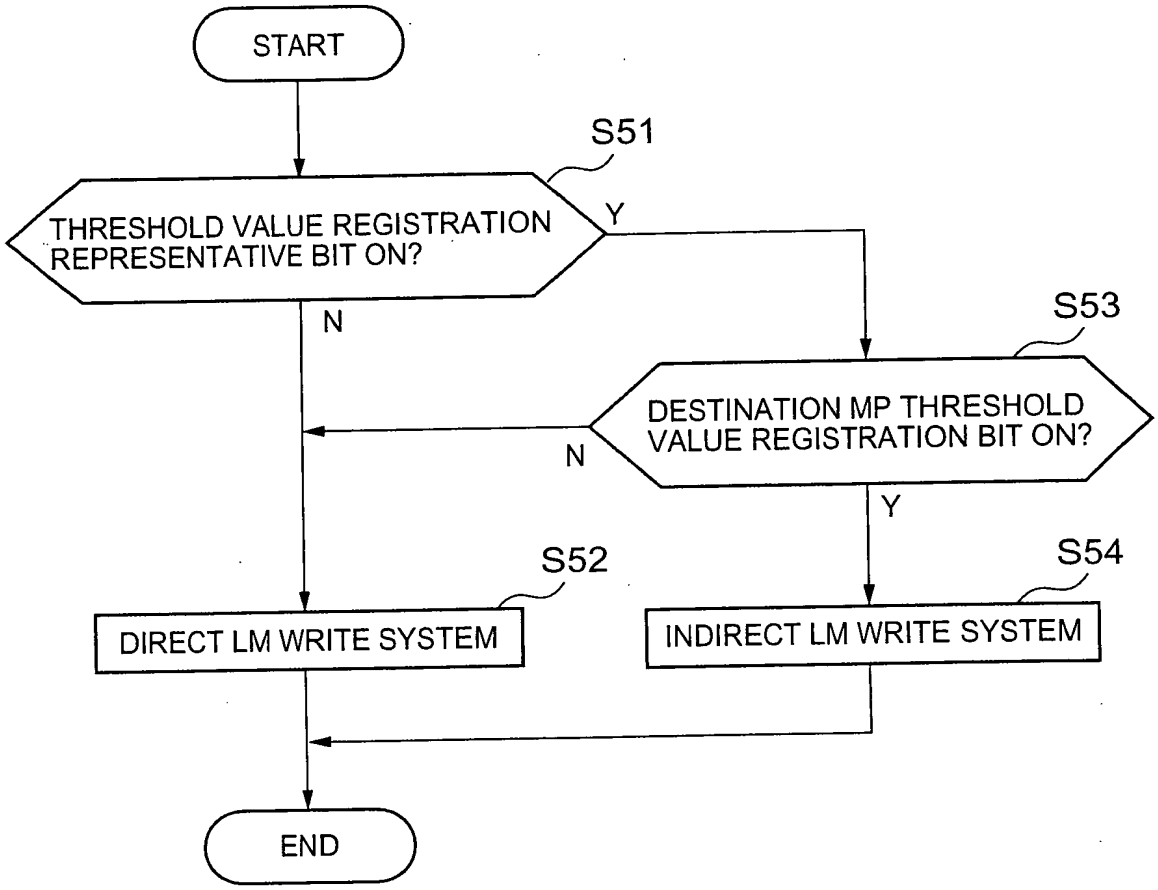

START
S51
THRESHOLD VALUE REGISTRATION REPRESENTATIVE BIT ON?
Y
N
S53
DESTINATION MP THRESHOLD VALUE REGISTRATION BIT ON?
N
Y
S52
S54
DIRECT LM WRITE SYSTEM
INDIRECT LM WRITE SYSTEM
END

FIG. 14

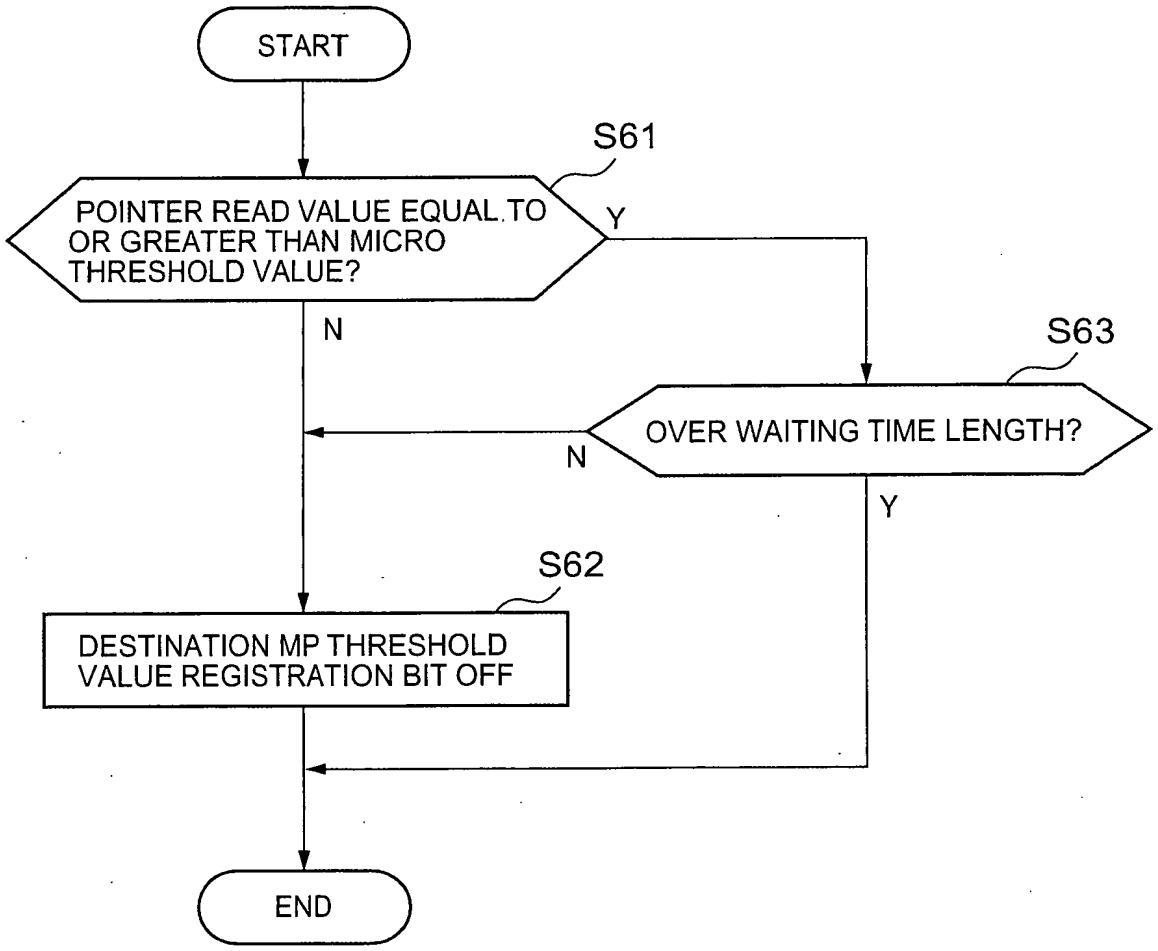

START
S61
POINTER READ VALUE EQUAL TO OR GREATER THAN MICRO THRESHOLD VALUE?
Y
N
S63
OVER WAITING TIME LENGTH?
N
Y
S62
DESTINATION MP THRESHOLD VALUE REGISTRATION BIT OFF
END

FIG. 15

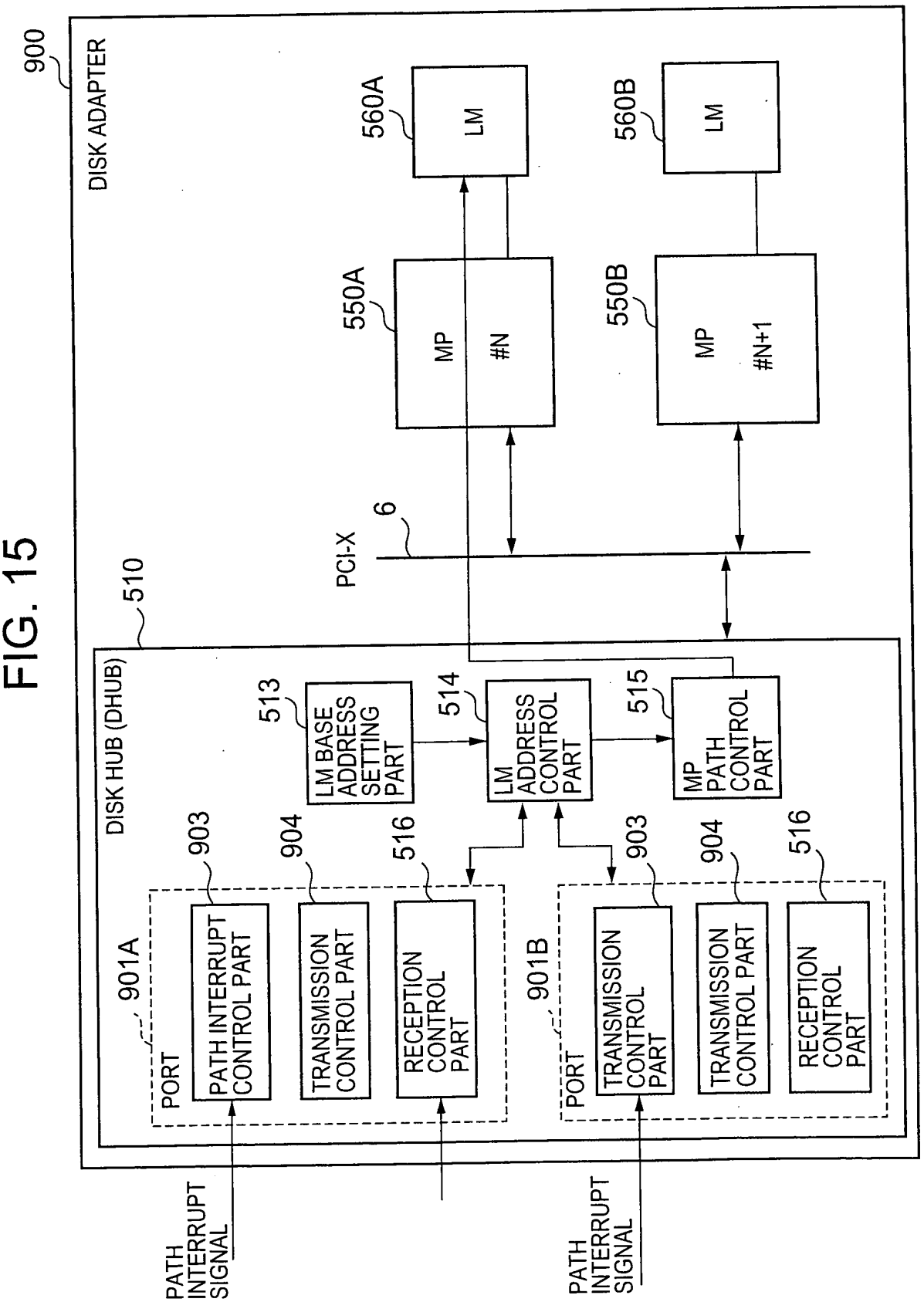

900
DISK ADAPTER
560A
LM
560B
LM
550A
MP
#N
550B
MP
#N+1
PCI-X
6
510
DISK HUB (DHUB)
513
LM BASE ADDRESS SETTING PART
514
LM ADDRESS CONTROL PART
515
MP PATH CONTROL PART
903
904
516
901A
PORT
PATH INTERRUPT CONTROL PART
TRANSMISSION CONTROL PART
RECEPTION CONTROL PART
901B
PORT
TRANSMISSION CONTROL PART
TRANSMISSION CONTROL PART
RECEPTION CONTROL PART
PATH INTERRUPT SIGNAL
PATH INTERRUPT SIGNAL

FIG. 16

ADDRESS INFORMATION (INT ADDRESS)
COMMAND TYPE (READ REQUEST)
CRC

FIG. 17

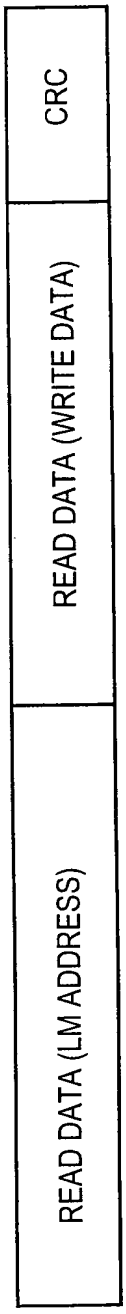

READ DATA (LM ADDRESS)
READ DATA (WRITE DATA)
CRC

FIG. 18

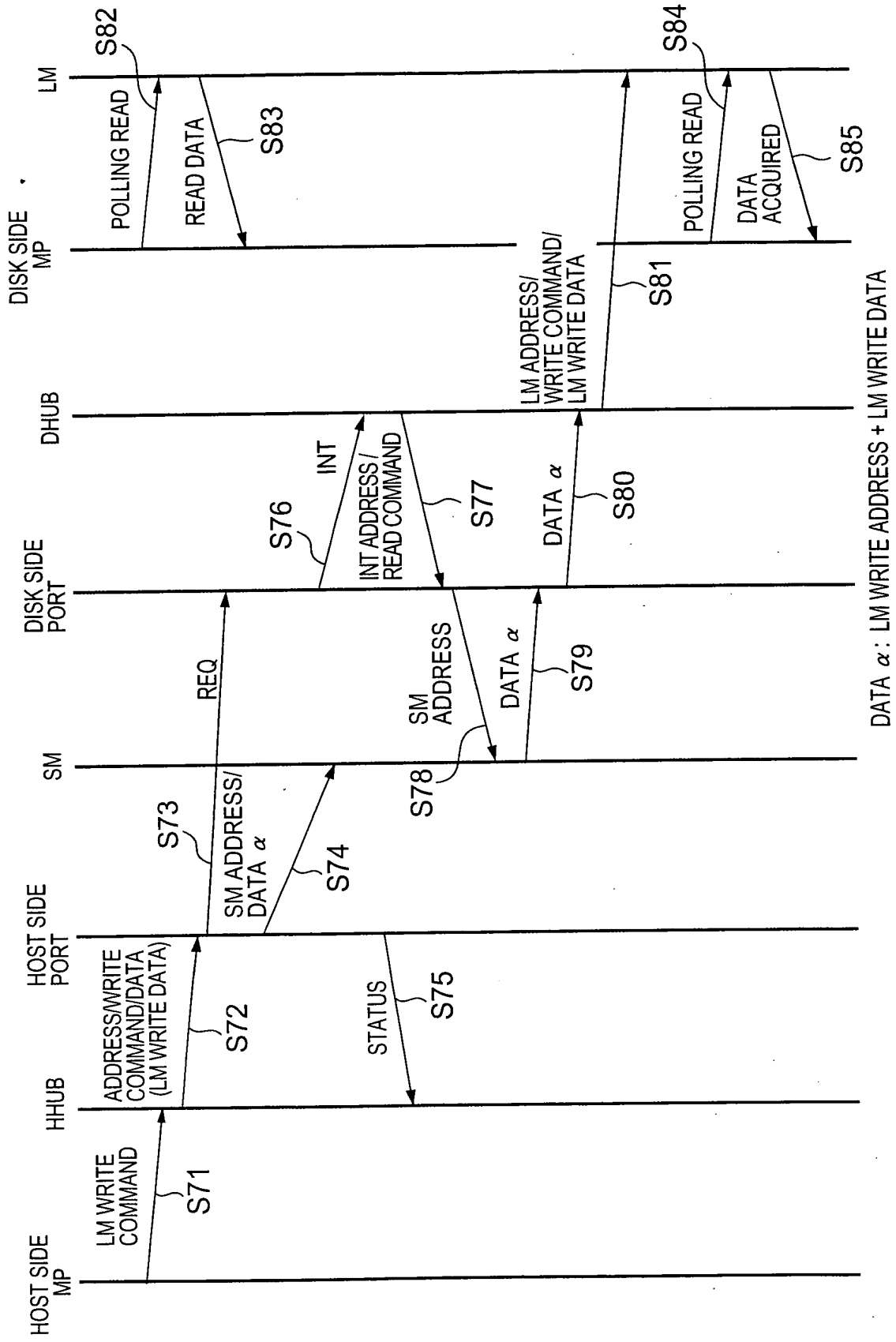

HOST SIDE MP
HHUB
HOST SIDE PORT
SM
DISK SIDE PORT
DHUB
DISK SIDE MP
LM
LM WRITE COMMAND
S71
ADDRESS/WRITE COMMAND/DATA (LM WRITE DATA)
S72
REQ
S73
SM ADDRESS/ DATA α
S74
STATUS
S75
INT
S76
INT ADDRESS / READ COMMAND
S77
SM ADDRESS
S78
DATA α
S79
DATA α
S80
LM ADDRESS/ WRITE COMMAND/ LM WRITE DATA
S81
POLLING READ
S82
READ DATA
S83
POLLING READ
S84
DATA ACQUIRED
S85
DATA α : LM WRITE ADDRESS + LM WRITE DATA

FIG. 19

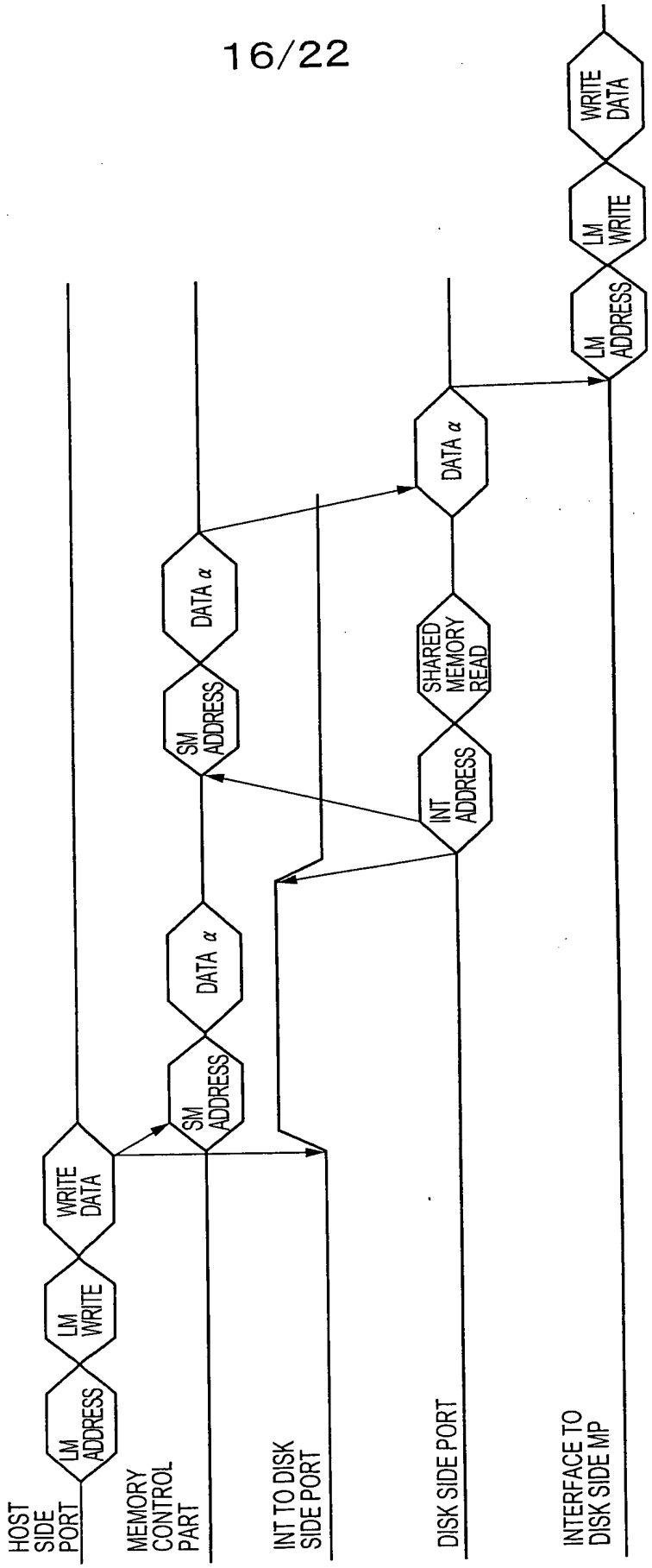

HOST SIDE PORT
MEMORY CONTROL PART
INT TO DISK SIDE PORT
DISK SIDE PORT
INTERFACE TO DISK SIDE MP
LM ADDRESS
LM WRITE
WRITE DATA
SM ADDRESS
DATA α
DATA α
SM ADDRESS
INT ADDRESS
SHARED MEMORY READ
DATA α
LM ADDRESS
LM WRITE
WRITE DATA

FIG. 20

MP360 (MP # "00")

ADDRESS	USE
0x0000 0000	PCIX OR OTHER DEVICE
0x1000 0000	SMA I/O REGISTER
0x2000 0000	TRANSMISSION SM ADDRESS INFORMATION
0x3000 0000	RECEPTION SM ADDRESS INFORMATION
0x4000 0000	LM WRITE ADDRESS INFORMATION FOR OTHER MP
0x5000 0000	LM WRITE/READ ADDRESS INFORMATION FOR OWN MP
0x6000 0000	LM READ ADDRESS INFORMATION FOR OTHER MP

12

START	NAME OF ADAPTER	OTHER MP #	OTHER LM WRITE ADDRESS
0x4000 0000	CHA0	00	0x0000 0000
0x4100 0000		01	0x0000 0000
0x4200 0000	CHA1	02	0x0000 0000
0x4300 0000		03	0x0000 0000
0x4400 0000	CHA2	04	0x0000 0000
0x4500 0000		05	0x0000 0000
0x4600 0000	CHA3	06	0x0000 0000
0x4700 0000		07	0x0000 0000
0x4800 0000	DKA0	08	0x0000 0000
0x4900 0000		09	0x0000 0000
0x4A00 0000	DKA1	0a	0x0000 0000
0x4B00 0000		0b	0x0000 0000
0x4C00 0000	DKA2	0c	0x0000 0000
0x4D00 0000		0d	0x0000 0000
0x4E00 0000	DKA3	0e	0x0000 0000
0x4F00 0000		0f	0x0000 0000

START	NAME OF ADAPTER	OTHER MP #	OTHER LM READ ADDRESS
0x4000 0000	CHA0	00	0x0000 0000
0x4100 0000		01	0x0000 0000
0x4200 0000	CHA1	02	0x0000 0000
0x4300 0000		03	0x0000 0000
0x4400 0000	CHA2	04	0x0000 0000
0x4500 0000		05	0x0000 0000
0x4600 0000	CHA3	06	0x0000 0000
0x4700 0000		07	0x0000 0000
0x4800 0000	DKA0	08	0x0000 0000
0x4900 0000		09	0x0000 0000
0x4A00 0000	DKA1	0a	0x0000 0000
0x4B00 0000		0b	0x0000 0000
0x4C00 0000	DKA2	0c	0x0000 0000
0x4D00 0000		0d	0x0000 0000
0x4E00 0000	DKA3	0e	0x0000 0000
0x4F00 0000		0f	0x0000 0000

FIG. 21

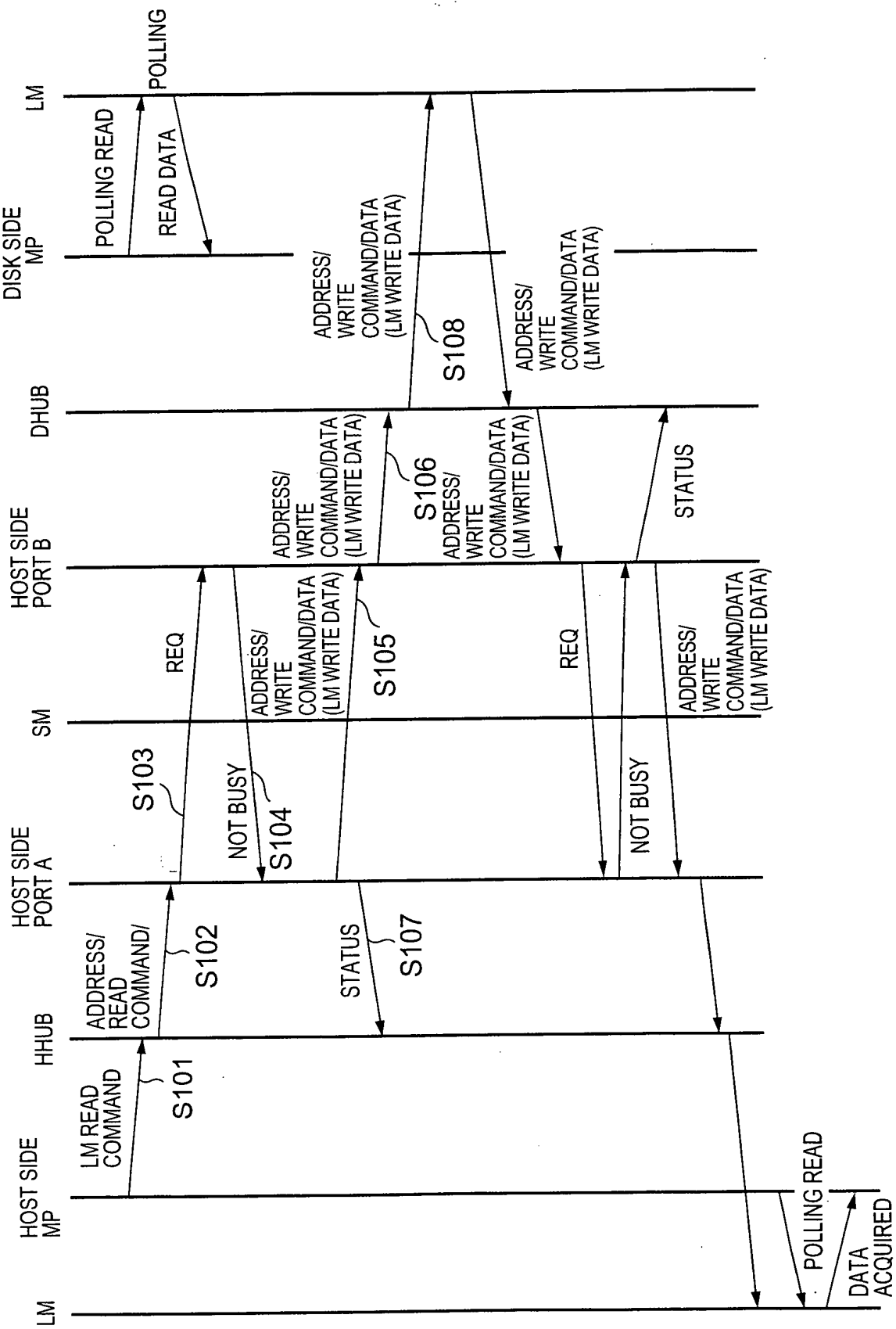

LM
HOST SIDE MP
HHUB
HOST SIDE PORT A
SM
HOST SIDE PORT B
DHUB
DISK SIDE MP
LM
LM READ COMMAND
ADDRESS/ READ COMMAND/
S101
S102
REQ
S103
NOT BUSY
S104
ADDRESS/ WRITE COMMAND/DATA (LM WRITE DATA)
S105
STATUS
S107
ADDRESS/ WRITE COMMAND/DATA (LM WRITE DATA)
S106
REQ
NOT BUSY
ADDRESS/ WRITE COMMAND/DATA (LM WRITE DATA)
STATUS
ADDRESS/ WRITE COMMAND/DATA (LM WRITE DATA)
S108
ADDRESS/ WRITE COMMAND/DATA (LM WRITE DATA)
POLLING READ
READ DATA
POLLING
POLLING READ
DATA ACQUIRED

FIG. 22

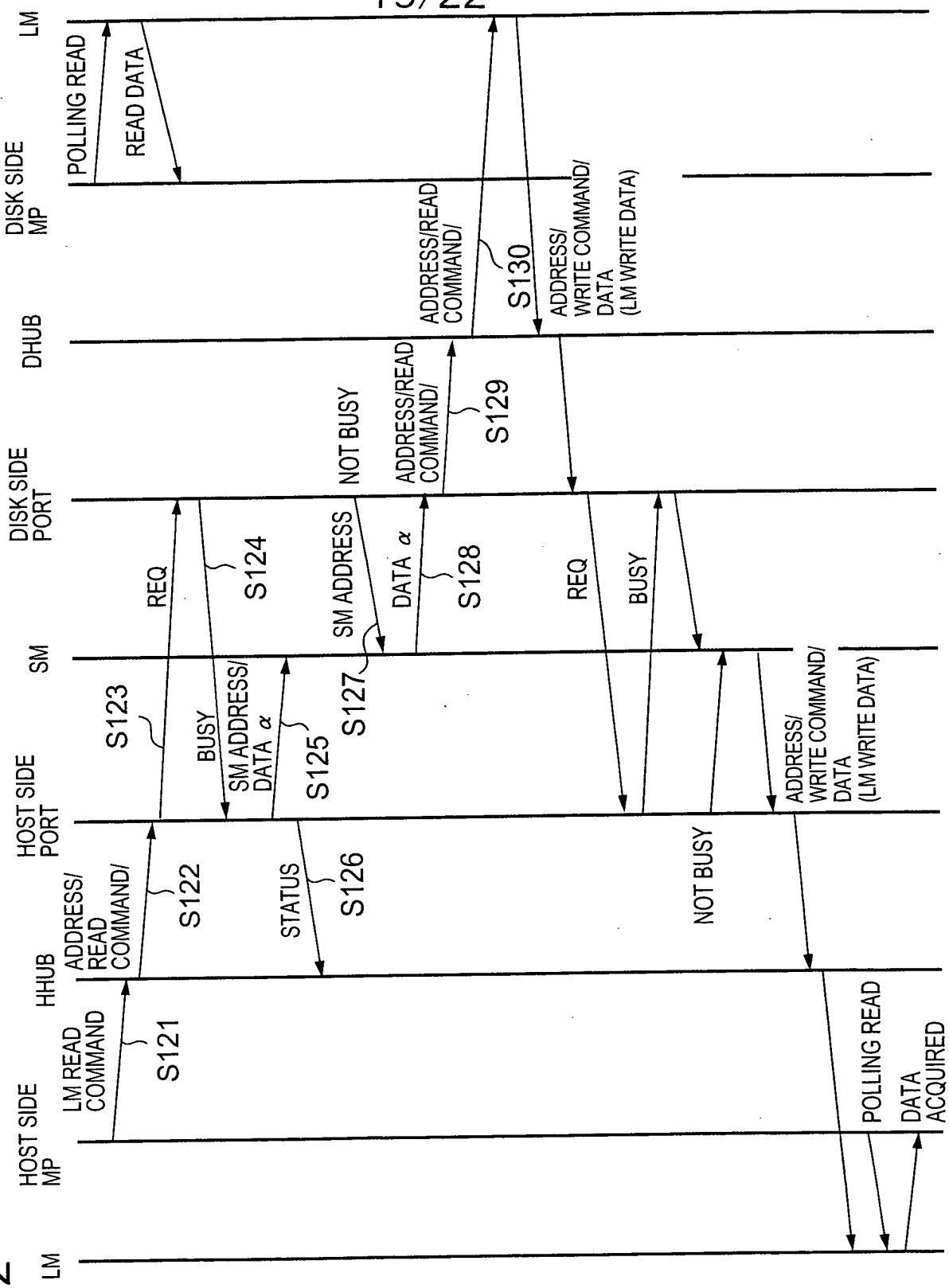

HOST SIDE MP
HHUB
HOST SIDE PORT
SM
DISK SIDE PORT
DHUB
DISK SIDE MP
LM
LM READ COMMAND
ADDRESS/ READ COMMAND/
REQ
BUSY
SM ADDRESS/ DATA α
SM ADDRESS
DATA α
NOT BUSY
ADDRESS/READ COMMAND/
ADDRESS/ WRITE COMMAND/ DATA (LM WRITE DATA)
POLLING READ
READ DATA
STATUS
DATA ACQUIRED
S121
S122
S123
S124
S125
S126
S127
S128
S129
S130

FIG. 23

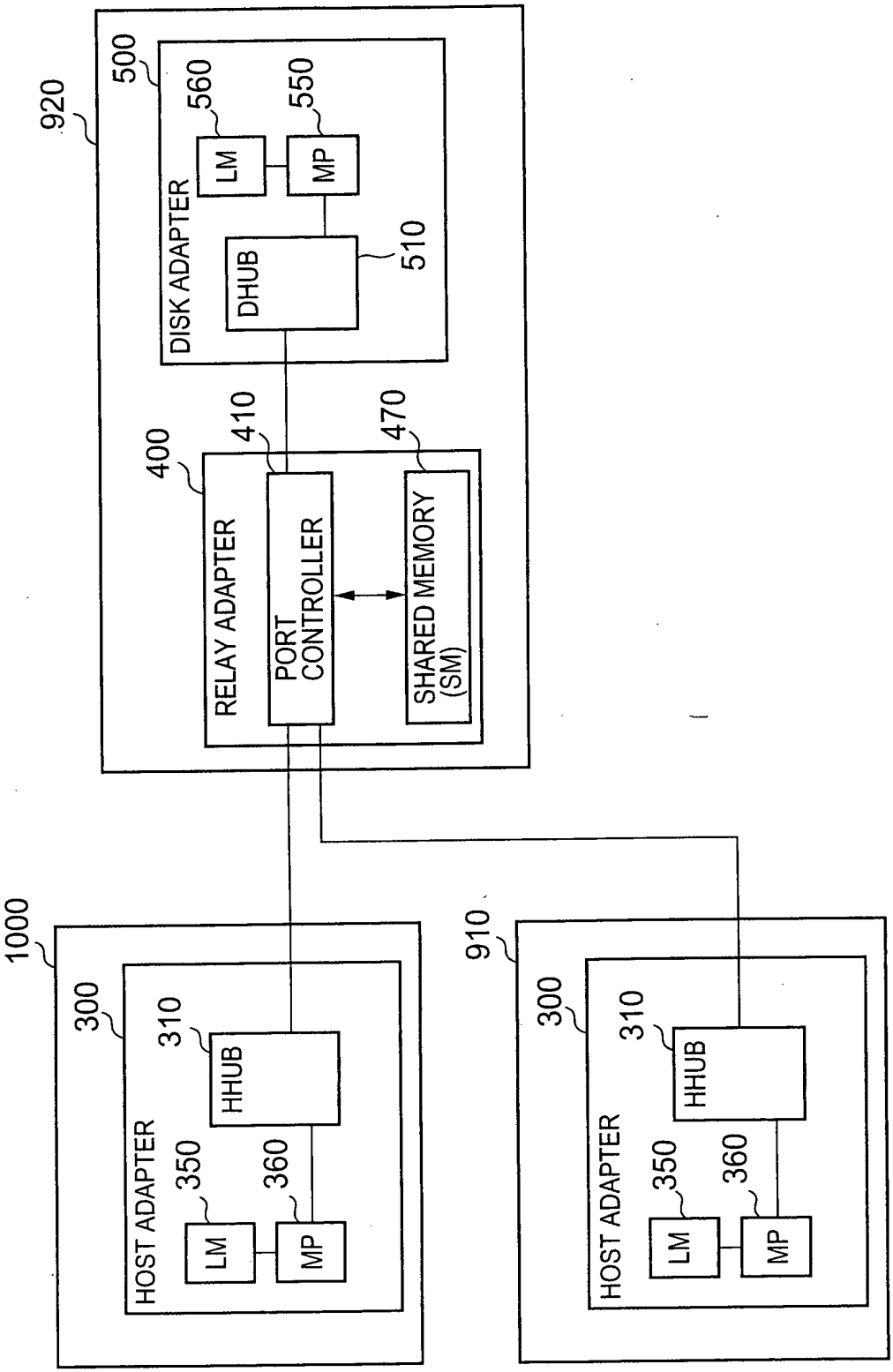

920
500
DISK ADAPTER
560
LM
550
MP
DHUB
510
400
410
RELAY ADAPTER
PORT CONTROLLER
470
SHARED MEMORY (SM)
1000
300
HOST ADAPTER
310
HHUB
350
LM
360
MP
910
300
HOST ADAPTER
310
HHUB
350
LM
360
MP

FIG. 24

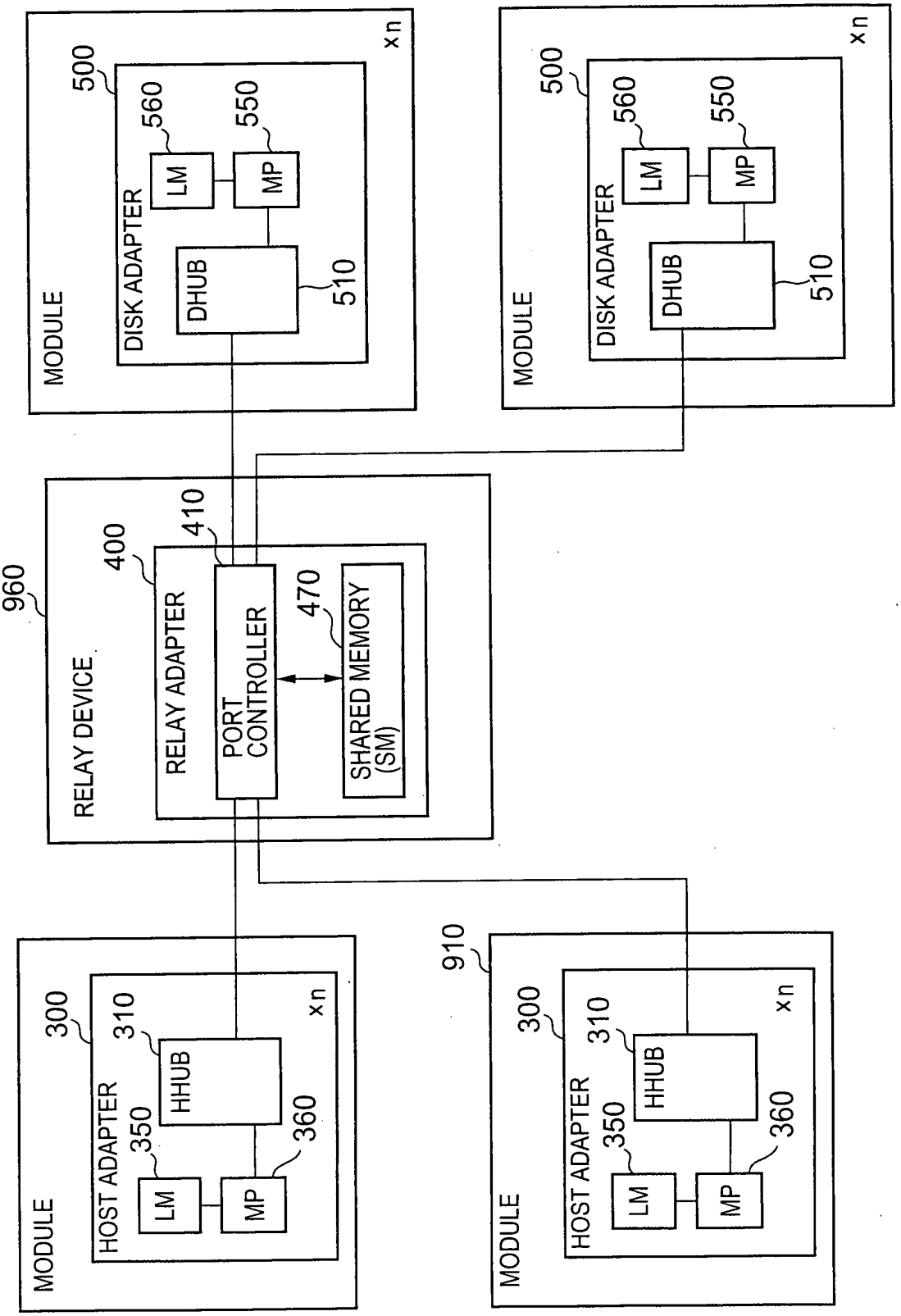
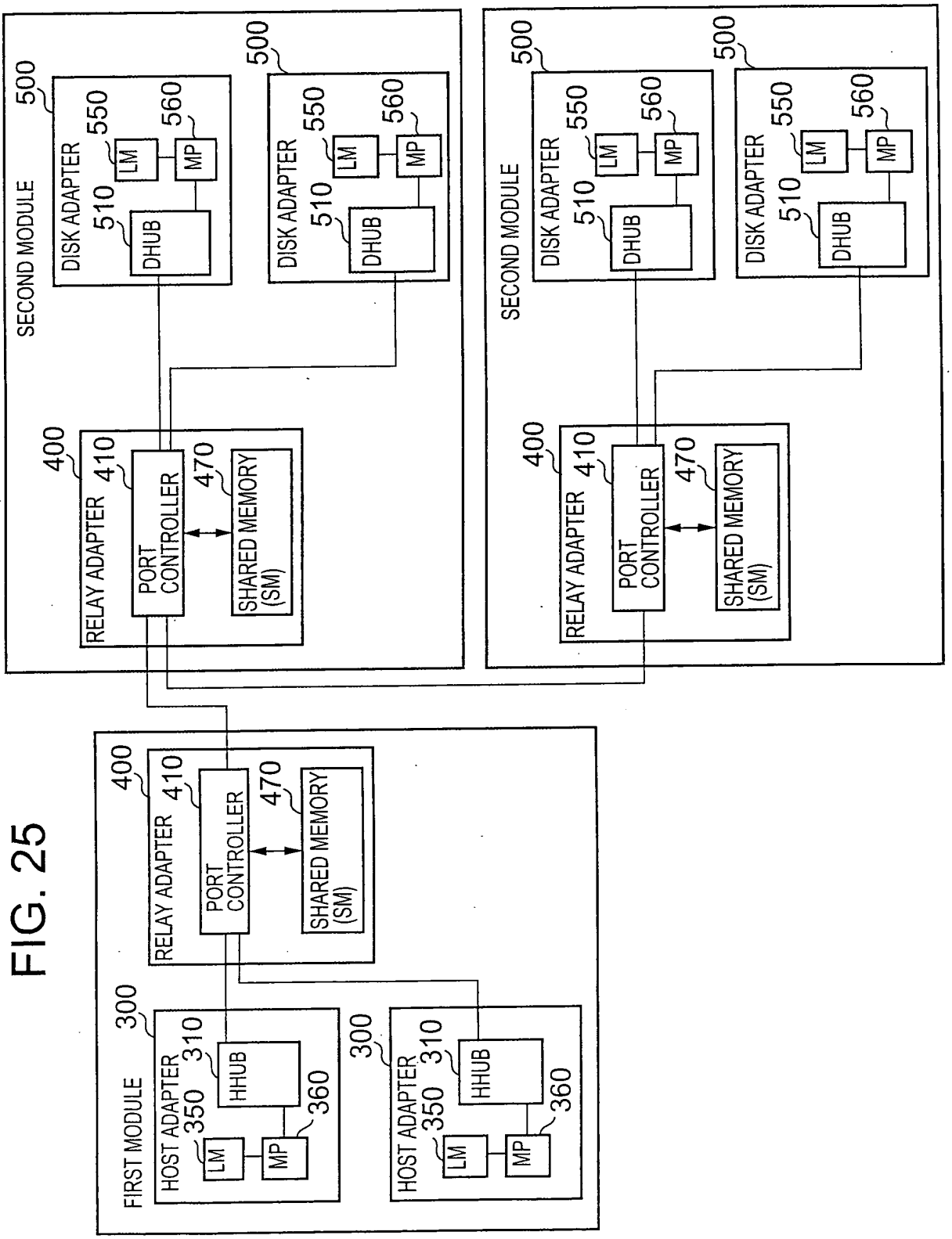

960
RELAY DEVICE
400
RELAY ADAPTER
410
PORT CONTROLLER
470
SHARED MEMORY (SM)
MODULE
500
DISK ADAPTER
560
LM
550
MP
DHUB
510
x n
910
300
HOST ADAPTER
310
HHUB
350
360

FIG. 25


SECOND MODULE
500
DISK ADAPTER
510
DHUB
550
LM
560
MP
400
RELAY ADAPTER
410
PORT CONTROLLER
470
SHARED MEMORY (SM)
FIRST MODULE
300
HOST ADAPTER
310
HHUB
350
360